REMARKS

Claims 1, 3, 4, 5, and 7 have been amended. Claims 21 - 22 have been added.

In response to the restriction requirement set forth in the December 7, 2000 Office Action, applicants elect, with traverse, for the continued prosecution of the species of Fig. 1. It is believed that claims 1 - 2, 5, 6, 9 - 10, 12, 14 - 19, 21, and 22 read on species of Fig. 1.

Applicants respectfully submit that claims 1- 2, 5, 6, 9 - 10, 12, 14 - 19, 21 and 22 are believed to be directed to the species of Fig. 1 and they may be searched and examined along with claims 3 -4, 7 -8, 11, 13, and 20, believed to be directed to the species of Fig. 8, without undue burden by the Examiner. More specifically, both sets of claims are directed to a common object of providing an input protection circuit having a high electrostatic discharge breakdown voltage and being capable of inputting positive and negative input signals in a broad input signal level range. Further, claim 9 and new claims 21 and 22 are believed to be generic claims covering the species of Fig. 1 and the species of Fig. 8.

Assuming, *arguendo*, that the species of Fig. 1 and Fig. 8 are distinct and independent inventions, the Manual of Patent Examining Procedure (MPEP) § 803 states that, "If the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to distinct or independent inventions." Based on the foregoing, it is respectfully submitted that claims 1 - 2, 5, 6, 9 - 10, 12, 14 - 19, 21, and 22 should be searched and examined along with claims 3 - 4, 7 - 8, 11, 13, and 20 to avoid unnecessary delay and expense to the applicant and duplicative examination by the Patent Office. Applicants

respectfully request that claims 1 - 2, 5, 6, 9 - 10, 12, 14 - 19, 21, and 22 and claims 3 - 4, 7 - 8, 11, 13, and 20 be prosecuted together in the same application.

Upon entry of this Election, claims 1-22 are pending.

Further action on the merits is respectfully requested.

Respectfully submitted,

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APPENDIX

Please amend claims 1, 3, 4, 5, and 7 and add new claims 21 and 22, as follows.

1. (Amended) An input protection circuit, [comprising] according to claim 21,

[an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate; and

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate,]

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, and said fourth well region and the base of the second lateral bipolar transistor are connected to [a] said reference potential node.

3. (Amended) An input protection circuit, [comprising] according to claim 21,

[an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of the first conductivity type formed in one principal surface area of said semiconductor substrate;

second and third well regions of a second conductivity type opposite to the first conductivity type, said second and third well regions being formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base, bottoms of said second and third well regions forming a PN junction with said first well or with said semiconductor substrate;

a fourth well region of the second conductivity type formed in the principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; and

first and second impurity doped regions of the first conductivity type formed in said fourth well region and forming a second lateral bipolar transistor with a portion of said fourth well region serving as a base,]

wherein said input terminal is connected to said third well region, said fourth well region and the base of said [first] second lateral bipolar transistor are connected to said first impurity doped region, and said second impurity doped region and the base of the [second] first lateral bipolar transistor are connected to [a] said reference potential node .

4. (Amended) An input protection circuit according to claim 3, further

comprising a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said [second] third well region.

5. (Amended) An input protection circuit, [comprising] according to claim 22,

[an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; and

second and third well regions of the second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base,]

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, and said third well region and the base of the second lateral bipolar transistor are connected to [a] said reference potential node.

7. (Amended) An input protection circuit, [comprising] according to claim 22,

[an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

first and second well regions of a second conductivity type opposite to the first conductivity type, said first and second well regions being forming on one principal surface area of said semiconductor substrate and forming a first lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a third well of the second conductivity type formed in the principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; and

first and second impurity doped regions of the first conductivity type formed in said third well region and forming a second lateral bipolar transistor with a portion of said third well region serving as a base,]

wherein said input terminal is connected to said [first] second well, said [second] third well region and the base of said [first] second lateral bipolar transistor are connected to said first impurity doped region, and said second impurity doped region and the base of the [second] first lateral bipolar transistor are connected to [a] said reference potential node.

21. (New) An input protection circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of

said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate,

an input terminal formed on said semiconductor substrate;

a circuit formed in said semiconductor substrate, and connected to said input terminal; and

a reference potential node formed on said semiconductor substrate;

wherein said first and second lateral bipolar transistors are connected in series between said input terminal and said reference potential node.

22. (New) An input protection circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of the second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

an input terminal formed on said semiconductor substrate;

a circuit formed on said semiconductor substrate, and connected to said input terminal; and

a reference potential node formed on said semiconductor substrate;

wherein said first and second lateral bipolar transistors are connected in series between said input terminal and said reference potential node.